REMARKS

Claims 1-20 were pending when last examined, all of which stand rejected. Applicant respectfully requests reconsideration and allowance of all the pending claims in light of the following remarks.

Drawings

Per Examiner's suggestion, new versions of FIGs. 8-11 and 13-15 with larger lettering will be submitted upon the allowance of the application. New versions of FIGs. 1-4 including the label "Prior Art" are submitted herewith.

Specification

The Abstract has been amended to eliminate the unclear phrase indicated by the Examiner. The acronym BCJR in paragraph [0009] has been defined in accordance with Examiner's suggestion. The specification has been amended to correct obvious grammatical errors.

Claim Objections

Although the Office Action objects to Claim 10, the content of the objection indicates that the objection should be directed at Claim 11. Thus, Claim 11 has been amended in accordance with the objection.

Claim Rejections -- 35 USC § 102

Claims 1-5, 9-12, 14-17, and 20 are rejected as being anticipated by USP 6,175,940 to Saunders ("Saunders").

Claim 1 is patentable over Saunders at least because it recites "*independently reconfigurable* processing elements for performing a turbo coding routine...." The Office Action cited Saunders' col. 2, lines 31-35 as teaching this recited element. However, the cited section of Saunders, which describes Saunders' FIG. 5, only mentions a conventional concatenated coding scheme and makes no reference to "*independently reconfigurable* processing elements." Even the description of FIG. 5 in Saunders' col. 4, lines 36-46 does not mention that the gate elements in the FPGA are independently reconfigurable.

Claims 2-5, 9, and 10 depend from Claim 1 and are patentable over Saunders for the same reasons as Claim 1.

Claim 9 is patentable over Saunders for the additional reason that it recites that "each processing element includes at least one functional unit ..." wherein the functional unit is programmed to perform at least one function of the turbo coding routine. The fact that each processing element in the array includes at least one functional unit stands in stark contrast with the FPGA array in Saunders, which *synthesizes* functions that may be integrated with existing encoding functions (see Saunders, col. 4, lines 36-41).

Claim 10 depends from Claim 9 and is therefore patentable over Saunders for at least the same reasons as Claim 9.

Claim 11 is patentable over Saunders at least because it recites, "an array of interconnected, reconfigurable processing elements, each processing element being independently programmable with a context instruction...." A processing element that is independently programmable with a context instruction is configured to perform a specific function according to a context. As described above, Saunders' array is a Field Programmable Gate Array, which is a type of hard-wired logic chip. The gate arrays are not "independently programmable with a context instruction."

Claim 11 is also patentable over Saunders because it recites "a context memory ... for storing and providing the context instruction to the processing elements...." Since Saunders' FPGA does not use context instructions, there is no context memory in Saunders' system.

Claims 12 and 14-17 depend from Claim 11 and are therefore patentable over Saunders for the same reasons as Claim 11.

Claim 17 is patentable over Saunders for the additional reason that it recites a "programmable logic that is configurable by the context instruction." Saunders' FPGA includes an array of logic element, and there is no indication that each logic element can be configured to perform a specific function according to a context. Thus, unlike the apparatus of Claim 17, the Saunders' system is not "configurable by the context instruction."

Claim Rejections – 35 USC § 103

Claims 6, 7, 13, and 19 are rejected under 35 USC § 103(a) as being unpatentable over Saunders in view of USP 6,813,742 to Nguyen ("Nguyen"). As these claims depend from Claim 10, they are all patentable over Shiogama for the same reasons as Claim 10.

Claims 6 and 7 depend from Claim 1 and each recites "an array of independently reconfigurable processing elements for performing a turbo coding routine...." As explained above, Saunders does not teach or suggest independently reconfigurable processing elements. Nor does Nguyen, which pertains to a baseband processor for processing sequences of received baseband digital signals. Since neither Saunders nor Nguyen teaches or discloses all the elements of Claim 1, Claim 1 is patentable over a combination of Saunders and Nguyen.

Claims 13 and 19 depend from Claim 11 and therefore each recites, "an array of interconnected, reconfigurable processing elements, each processing element being independently programmable with a context instruction..." and "a context memory ... for storing and providing the context instruction to the processing elements...." As explained above, Saunders does not teach or suggest these elements. Nguyen, which discloses a baseband processor for turbo code decoding, does not teach an array of processing elements of any type. Nguyen does not mention using a context instruction, and therefore does not teach or suggest using a context memory for storing and providing any context instruction. Thus, Saunders and Nguyen, even in combination, do not disclose all the elements of Claims 13 and 19, and Claims 13 and 19 are patentable over Saunders and Nguyen.

Claims 8 and 18 are rejected as being unpatentable over Saunders in view of USP 6,484,283 to Stephen et al ("Stephen").

Claim 8 is patentable over Saunders and Stephen at least because it depends from Claim 1 and recites, "an array of independently reconfigurable processing elements for performing a turbo coding routine...." As explained above, Saunders does not teach the recited type of array. Stephen, which discloses turbo encoder/decoder, does not disclose using an array of independently reconfigurable processing elements. Thus, Saunders and Stephen, even in combination, do not teach or suggest all the elements of Claim 8.

Claim 8 is further patentable over Saunders and Stephen because it recites "idling all processing elements in the array other than the portion of processing elements configured for performing the turbo coding routine." Although the Office Action cites to Stephen's col. 31, lines 4-23 as teaching this element, the cited section does not disclose idling a part of the array.

First of all, there is no array of processing elements in the cited section. The "idling" referred to in the cited section refers to the idling of a controller in the SISO module, neither of which is indicated to include an array. Given that there is no array, Stephens cannot teach or suggest "idling all processing elements in the array other than the portion [that is] configured for performing the turbo coding routine."

Claim 18 is patentable over Saunders and Stephen because it depends from Claim 11, which recites "an array of interconnected, reconfigurable processing elements, each processing element being independently programmable with a context instruction," and "a context memory ... for storing and providing the context instruction to the processing elements." There is no mention in Saunders or Stephen of processing element that is "independently programmable with a context instruction." Given that there is no mention of context instruction, there is no need for a context memory that stores the context instruction. Thus, Saunders and Stephen, even in combination, do not disclose all the elements of Claim 18.

Claim 18 is further patentable over Saunders and Stephen because it recites that the processor is "configured to idle all processing elements that are not of the portion of processing elements configured for performing the turbo coding routine." While the Office Action cited to Stephen's col. 31, lines 4-23 as teaching this element, the cited section does not even mention an array of processing elements. Given that there is no array of processing elements, Stephen cannot teach or suggest a processor that is configured to idle a portion of the array.

Conclusion

Based on the foregoing reasons, Claims 1-19 are in condition for allowance. Please telephone the undersigned attorney at (650) 833-2121 if there are any questions.

Respectfully submitted,

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Amendments to the Drawings:

The attached sheets of drawings include changes to FIGs. 1-4 and replace the original FIGs. 1-4. In accordance with the Examiner's request the label "Prior Art" has been added to FIGs. 1-4.

Attachment: Replacement Sheet